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Declarations under Rule 4.17:
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(54) Title: WAFER LEVEL INTERCONNECTION

(57) Abstract: RF MicroElectroMechanical Systems (MEMs) circuitry (15) on a first high resistivity substrate (17) is combined with circuitry (11) on second low-resistivity substrate (13) by overlapping the first high resistivity substrate (17) and MEMs circuitry (15) with the low resistivity substrate (13) and circuitry (11) with the MEMs circuitry (15) facing the second circuitry (11). A dielectric lid (19) is placed over the MEMs circuitry (15) and between the first substrate (17) and second substrate (13) with an inert gas in a gap (21) over the MEMs circuitry (15). Interconnecting conductors (25, 31, 35, 37, 39, 41) extend perpendicular and through the high resistivity substrate (17) and through the dielectric lid (19) to make electrical connection with the low resistivity substrate (13).

WAFER LEVEL INTERCONNECTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to RF MEMS (MicroElectroMechanical Systems) technology and more particularly to MEMS with wafer level interconnection to electronics on low-resistivity substrate material.

2. Background of Invention

RF MEMS technology has been targeted for insertion in a wide range of military applications from multi-band multi-mode communication systems to inertial navigation systems to sensors. In fact, RF MEMS technology insertion plays a major role in numerous current DARPA funded programs such as Ultra Comm and the Airborne Communications Node (ACN).

This technology could be applied to these programs plus new military insertion opportunities such as targeting systems, satellite communications, high speed tactical data link systems, electronic warfare and countermeasure systems, signal intelligence systems, and antenna systems.

This technology could also be applied to consumer electronics applications such as telecommunications (cellular telephone, back-haul, etc.) commercial aircraft, commercial radar, etc. where the distinct performance advantages and small form factor provided by the combination of RF MEMS and silicon germanium (SiGe) or other electronic circuits are desired.

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silicon germanium (SiGe) or other electronic circuits are desired.

Many hetero-junction technologies, epitaxial methods, and substrate materials have been considered incompatible. Specifically, RF MEMS fabrication technology has been considered incompatible with silicon germanium (SiGe) fabrication technology. RF MEMS technology requires a high resistivity substrate material to maximize the circuit RF performance. Typically SiGe circuits are processed on low resistivity material.

Raytheon has investigated the integration of RF MEMS circuitry on a low resistivity SiGe substrate using a "direct integration" (DI) approach. The primary technical challenge associated with direct integration RF MEMS circuitry with sophisticated electronics is overcoming the influence of the low-resistivity substrate material, typically used by SiGe manufacturers, on the insertion loss of the RF MEMS circuit.

Direct integration (DI) was investigated by Raytheon for overcoming the detrimental affects of the low-resistivity substrate on microwave circuitry. DI involves building a second dielectric layer on top of the substrate to serve exclusively as the microwave substrate. DI, however, has a number of technical challenges.

RF MEMS circuits produced by Raytheon require a smooth substrate. This is necessary due to the geometry of the structures being produced. The flatness of the dielectric material for the DI approach is currently unknown. Secondly, the RF performance of the circuit can be limited by the thin microwave dielectric layer.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention wafer level interconnect removes the requirements

for substrate material as an issue. Each technology processes their circuitry on the required base material and minimizes the need for additional process development. Following initial processing, the two wafers are electrically interconnected with vertical electrical interconnections.

The wafer level interconnect invention will enable the integration of these two (and other) technologies where previously integration through wafer fabrication has been limited by a requirement for differing base substrate materials. This invention may also provide benefits for wafer level packaging of integrated circuits on silicon substrates where the
electrical signal must be isolated from the substrate.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross sectional sketch illustrating the subject invention according to one embodiment.

DESCRIPTION OF PREFERRED EMBODIMENTS

According to one embodiment of the present invention illustrated in Figure 1 vertical electrical interconnection between the electronics circuitry 11 on one low-resisitvity SiGe substrate 13 and RF MEMS circuitry 15 on a separate high resistivity silicon (HR) substrate 17. The low-resistivity substrate material 13 may also be ,silicon CMOS or gallium arsenide (GaAS) substrate. This is accomplished by using wafer fabrication techniques to construct a conductive metallization layer on either the primary (i.e., RF MEMS) substrate 17 or the secondary (i.e., other electronics) substrate 13. A dielectric lid 19 is spaced between the electronics circuitry 11 on the substrate 13 and the high resistivity substrate 17 and provides a canopy or lid over the RF MEMS circuitry 15 leaving a gap 21 over the RF MEMS

circuitry 15. The gap 21 is filled with an inert environment such as a gas such as nitrogen or a vacuum. The lid 19 may be made of Pyrex,quatrz or glass and is made of a material with the same coefficient of thermal expansion as the HR substrate material 17.

The interconnection 23 includes an input /output pin terminal 27 (such as a solder ball) and a first conductive via 25 through the HR silicon substrate 17 to a conductive pad 29 on the HR substrate 17 and a second conductive via 31 through the dielectric lid 19 to a conductive pad 33 of the electronic circuitry 11 on the low resistivity substrate 13. Solder or other conductive connecting means 30 may be used to connect the opposite ends of via 31. The conductive via 25 is insulated from the HR silicon 17 by an insulating oxide. Another conductive via 35 extends from the electronic circuitry 11 down through lid 19 and conductive connecting means 30 to the RF MEMs circuitry 15 at conductor 45. There may be a connection back up to the electronics 11 through a conductive via 37 and connecting means such as solder 30 from the RF MEMs circuitry 15 back up to the electronics circuitry 11 through the dielectric lid 19. A dielectric lid (not shown) may also be over the circuitry 11 between the circuitry 15 and circuitry 11 leaving a gap 22. The dielectric lid 19 may provide both gaps.

Further, as shown, there are conductive vias 39 and 41 that extend through dielectric lid 19 and HR silicon 17 to input/output pin terminal 43. The conductive via 41 is also insulated from the HR silicon 17 by an insulating oxide. This interconnection is like that of vias 25 and 31 with solder or other connecting means 30 on either end of via 39. There may also be a connection not shown from the circuitry 15 directly to the output terminal through via 41. The terminals 27 and 43 may be surface mounted and connected to a printed circuit

board. Using wafer level packaging techniques the secondary and primary substrates would then be bonded together to form both RF and DC electrical interconnections at the desire locations.

The RF MEMS circuitry 15 may be, for example, many switches like that as illustrated in the drawing for switching capacitance values. Switches A and B are illustrated. The switches A and B include a metal membrane 15a between supports 15b and 15c and a dielectric pad 15d under the membrane between the supports. When a control signal is applied, the membrane 15a contacts the dielectric pad 15d changing the capacitance value. For example, the value changes from 30 femtofarads(ff) with the unbent membrane to 3 picofarads (pf) with the membrane touches the dielectric pad 15d. The controls signals and RF from the electronics circuitry 11 are applied through the interconnecting via 35 and along connector 45 of circuitry 15 to switch A, along conductor 47 of circuitry 15 to switch B and from switch B along connector 49 of circuitry 15 to an output. In one embodiment by a connection (not shown) to via 41 to terminal 43. In another embodiment via 37 and connecting means 30 back to circuitry 11 and output from circuitry 11 or to terminal pin 43 through connector via 41 and connecting means 30. There may be a hermetic seal between the substrate 13 and the dielectric lid 19.

In the operation of the system RF and DC are applied at terminal 27. The RF and DC are applied to the electronics circuitry 11 through vias 25 and 31. The control signal for the RF MEMS switches A and B are applied through via 35 to cause the appropriate MEMs to switch capacitance. The RF signal from the electronic circuitry 11 is applied through via 35 to connector 45 and propogated through the switches A and B to the input/output pin 43 or other outputs (not shown) as discussed above.. The electronics circuitry 11 may include an

amplifier and the input to or output from the amplifier is filtered according to the capacitance values determined by the MEMS switches such as switches A and B.

Based upon past reviews of literature relating to wafer fabrication and *RF* MEMS, RF MEMS technology has never before been integrated with integrated circuits fabricated on a separate wafer. Furthermore, no article: have been observed relating to vertical electrical interconnection of two wafers using wafer fabrication techniques.

CLAIMS

What is claimed is:

1. In combination: a first substrate of high resistivity material having first circuitry thereon; a second substrate of low resistivity material having second circuitry thereon overlappingly spaced over said first substrate and facing said first circuitry; and interconnecting conductors extending perpendicular to said substrates between said first circuitry on said first substrate and second circuitry on said second substrate.

2. The combination of Claim 1 wherein said low resistivity material is silicon germanium (SiGe) ,silicon or gallium arsenide (GaAS).

3. The combination of Claim 2 wherein said high resistivity material is high resistivity silicon.

4. The combination of Claim 1 wherein said high resisitivity material is high resisitivity silicon.

5. The combination of claim 1 wherein said circuitry on said high resistivity material includes a MEMS structure.

6. The combination of Claim 1 wherein a dielectric lid is spaced between said first circuitry and said second circuitry and separating said first and second substrates.

7. The combination of Claim 6 wherein said dielectric lid is a glass, Pyrex or quartz lid.

8. The combination of Claim 6 wherein said interconnections extend through said lid.

9. The combination of Claim 8 wherein said lid is a dielectric lid presenting a gap over said first circuitry.

10. The combination of Claim 9 wherein said gap contains an inert environment.

11. The combination o Claim 10 wherein said inert invironment is nitrogen gas.

12. The combination of Claim 10 wherein said inert environment is a vacuum.

13. The combination of Claim 8 including said interconnecting conductors through said high resistivity material.

14. A method of interconnecting a first circuit on a high resistivity substrate to a second circuit on a low resistivity substrate comprising the steps of: placing a dielectric lid structure over said first circuit on said high resisitivity substrate leaving a gap over said first circuit ,overlapping said dielectric lid with said second circuit and said low resisitivity second substrate with said first circuit facing said second circuit and connecting said first circuit to said second circuit using interconnecting conductors extending perpendicular to said substrates and through said dielectric lid.

15. The method of Claim 13 wherein said low resistivity substrate is SiGe, silicon or GaAs.

16. The method of Claim 13 wherein said first circuitry includes MEMS circuitry.

17. The method of claim 15 wherein said said gap contains an inert gas.

18. The method of Claim 16 wherein said lid is of Pyrex material.

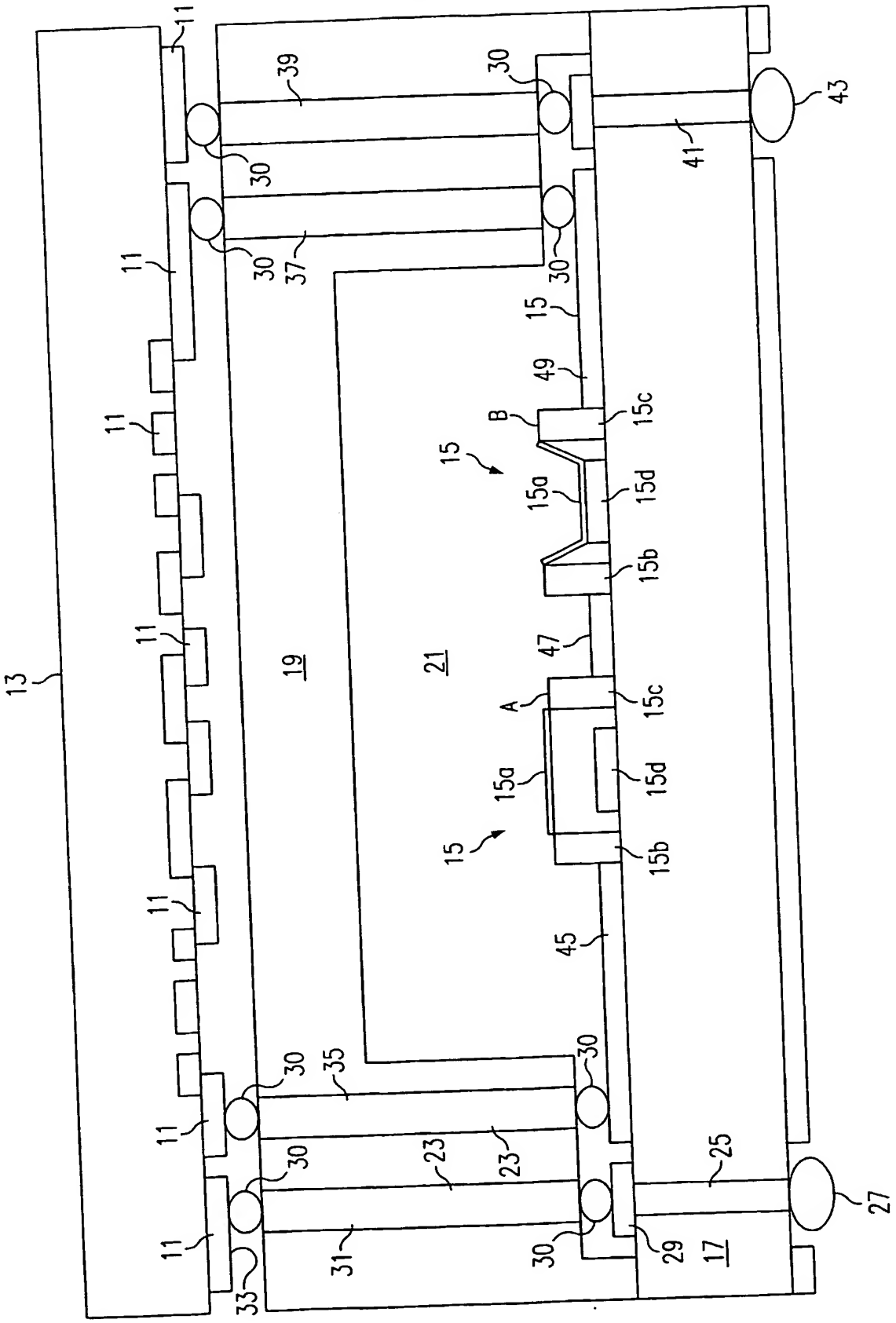
19. The method of Claim 16 wherein said lid is of glass material.

20. The method of Claim 16 wherein said lid is of quartz material.

21. The method of Claim 13 wherein said substrate is of SiGe material.

22. The combination of Claim 8 wherein said lid is a dielectric lid presenting a gap over said second circuitry.

23. The combination of Claim 8 wherein said lid is a dielectric lid presenting a gap over said first and second circuitry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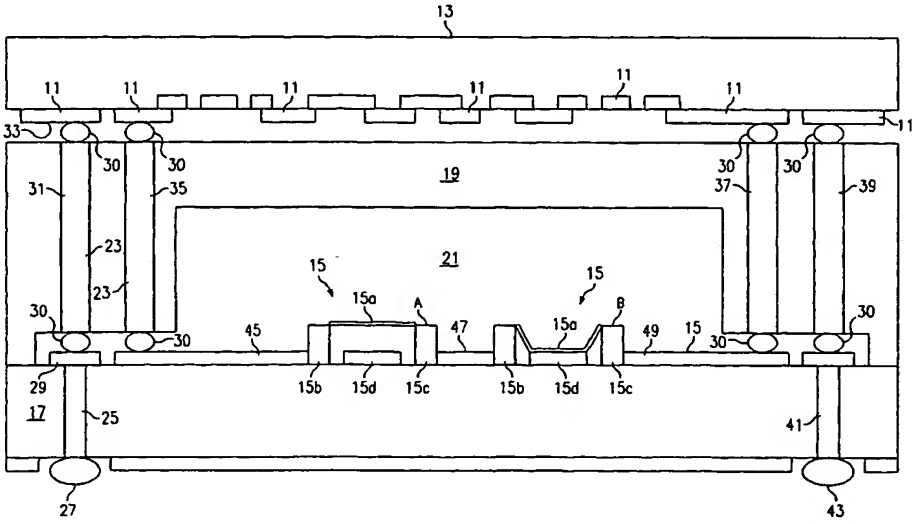
(54) Title: WAFER LEVEL INTERCONNECTION



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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B81B H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 825 284 A (SOGA TASAO ET AL) 25 April 1989 (1989-04-25) figures 2,3B,5F,9A column 5, line 60 -column 6, line 58	1,2,6,8, 9,13-15, 22,23
A		3-5,7, 10-12, 16-21

X	US 5 164 328 A (DUNN WILLIAM C ET AL) 17 November 1992 (1992-11-17) figures 1,2 column 1, line 56 -column 3, line 12	1,2,5
A		3,4,6-23

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
21 August 2002	28/08/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Polesello, P

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 100 27 234 A (AUSTRIA MIKROSYSTEME INT) 7 December 2000 (2000-12-07) figure 1 column 3, line 23 - line 51	1,2,5
A	---	3,4,6-23
X	FR 2 780 200 A (COMMISSARIAT ENERGIE ATOMIQUE) 24 December 1999 (1999-12-24) figure 9 page 14, line 10 - line 22	1,2
A	---	3-23
A	WO 97 12397 A (TEXAS INSTRUMENTS INC) 3 April 1997 (1997-04-03) figures 2-8,10 page 4, line 6 -page 5, line 6 page 16, line 16 -page 19, line 6 page 19, line 25 - line 30	1,6,8,14

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/50411

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4825284 A	25-04-1989	JP 62136865 A	19-06-1987
US 5164328 A	17-11-1992	JP 6013426 A	21-01-1994
DE 10027234 A	07-12-2000	AT 3609 U1	25-05-2000
		DE 10027234 A1	07-12-2000
FR 2780200 A	24-12-1999	FR 2780200 A1	24-12-1999
		EP 1090419 A1	11-04-2001
		WO 9967818 A1	29-12-1999
WO 9712397 A	03-04-1997	AU 703591 B2	25-03-1999
		AU 7393296 A	17-04-1997
		BR 9606658 A	04-11-1997
		CA 2205810 A1	03-04-1997
		CN 1165584 A	19-11-1997
		EP 0811245 A1	10-12-1997
		JP 10513611 T	22-12-1998
		WO 9712397 A1	03-04-1997